Register Number:

Date:



**ST. JOSEPH’ COLLEGE (AUTONOMOUS), BANGALORE - 27**

**SEMESTER EXAMINATION – APRIL 2020**

**B.Sc. Electronics – IV Semester**

**EL418: Verilog HDL**

**Time: 90 Minutes Max. Marks: 35**

Note: The question paper has three parts and one printed pages.

**PART – A**

**Answer any THREE of the following 03X05=15**

1. Define HDL? Discuss the four levels of design abstraction in Verilog.

2. Write a note on delays in gate level modeling.

3. Discuss time based delay control in behavioral modeling with proper example.

4. Write a note on looping statements used in behavioral modeling.

5. Write any five differences between tasks and functions.

**PART – B**

**Answer any THREE of the following 03X06=18**

6. a. Write a gate level design module for a 1-bit full adder.

b. Write a gate level design module for RS flip flop.

7. Write a design module for the following circuit. Draw the output timing diagram for a, b, c, e, and out.



The test conditions are as follows:

A= 1'b0; B= 1'b0; C= 1'b0;

#10 A= 1'b1; B= 1'b1; C= 1'b1;

#10 A= 1'b1; B= 1'b0; C= 1'b0;

#20 $finish;

8. Write a design (data flow) and test module for a 2 bit comparator.

9. Write a design module (using case statement) and test module for 1 to 4 demultiplexer.

10. a. Write a module using always and initial statements to design a clock with time period = 10 and duty cycle = 40%. Initial value of clock = 0.

b. Write a module using repeat loop to delay the statement a = a+1 by 20 positive edges of clock.

**PART – C**

**Answer any TWO of the following 02X01= 02**

11. What is the advantage of connecting ports by names over connecting ports by ordered list?

12. What is inertial delay?

13. Write two differences between sequential and parallel blocks.

14. Name two circuits which are examples of structural modeling.