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Register Number:

DATE: 13.04.2019

**ST. JOSEPH’S COLLEGE (AUTONOMOUS), BANGALORE-27**

**B.Sc. ELECTRONICS – IV SEMESTER**

**SEMESTER EXAMINATION- APRIL 2019**

**EL 415- VERILOG HDL**

**Time: 1 ½ hrs Maximum marks: 35**

This question paper has **TWO** printed pages and **THREE** parts.

**PART – A**

**ANSWER ANY THREE OF THE FOLLOWING 3X5=15 Marks**

1. a) Define a module? What do you understand by instantiation of gates in a module?

b) Draw and explain the top-down design hierarchy of a 4 bit Ripple Carry Counter. (2+3)

2. Explain the types of gate delays with example.

3. With example explain all bitwise operators.

4. Explain always statement with example

Explain general syntax of a case statement. (3+2)

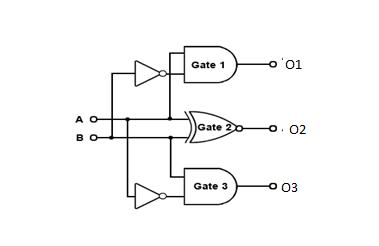
5. Write any FIVE differences between task and functions.

**PART – B**

**ANSWER ANY THREE OF THE FOLLOWING 3x6=18 Marks**

6. Write design (gate level) and test module for Full subtractor.

7. Write a design and test module for the following circuit.



8. Write a Verilog design and test module for JK Flip-Flop.

9. Write a Verilog design and test module to implement four bit ripple carry adder.

10. a. Write a module using always and initial statements to design a clock with time period = 40 and duty cycle = 25%. Initial value of clock = 0.

b. Write a module using repeat loop to delay the statement a = a+1 by 20 positive edges of clock.

**PART – C**

**ANSWER ANY TWO OF THE FOLLOWING 2x1=02 Marks**

11. What are the symbols used for representing an unknown value and a high impedance value?

12. Why ‘input’ cannot be declared as reg?

13. Mention all types of looping statements used in Verilog.

14. Name any two data types which can be declared under generate scope.

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