**ST.JOSEPH’S COLLEGE (AUTONOMOUS), BANGALORE – 27**

B.Sc. ELECTRONICS – IV SEMESTER

SEMESTER EXAMINATION – April 2018

**EL 415: Verilog HDL**

**Time : 1½hrs Maximum marks : 35**

Note: This question paper has two printed pages and three parts.

**PART – A**

**Answer any THREE of the following 03x05=15**

1. Explain the following “Lexical conventions” with examples.
	1. Comments b. Concatenation and Replication Operator c. Bitwise operator

 (2+2+1)

1. What is a module? Discuss the four levels of design abstraction used in a module.
2. Explain the continuous assignments in verilog with examples.
3. Explain the while and for loop statements in Verilog with examples.
4. Write any five differences between tasks and functions.

**PART – B**

**Answer any THREE of the following 03x06=18**

1. Write a Verilog design (using dataflow model) and test code to implement 1 bit full adder. Write its truth table.
2. Write a Verilog design module and test module for 1x4 DeMultiplexer.
3. Write a Verilog design module(behavioral) and test module for JK flipflop with reset input.

9. Write the design module, test module and draw the timing diagram to realize the output of the following.



 The above circuit is simulated using the following conditions:

 a=0, b=0, c=0

 #10 a=1, b=1, c=1

 #10 a=1, b=0, c=0

 #20 finish

1. a) Write a module called test. Declare a register called clock. Initialize it to 0. Using forever loop make it toggle every 30 time units.

b) Design a clock with time period = 40 and a duty cycle of 25% by using the always and initial statements. The value of clock at time = 0 should be initialized to 0. (3+3)

**PART – C**

**Answer any TWO of the following 02x01=02**

1. In the verilog statement and #(4,8) (y,a,b), what is the turn off delay?
2. Write two differences between initial and always statements.
3. Given: A = 4’b1xzz , B = 4’b1xzz , C = 4’b1xxz. Determine the result when A===B and A===C.
4. How use of generate statement helps in Verilog HDL?