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Register Number:

DATE:

**ST. JOSEPH’S COLLEGE (AUTONOMOUS), BENGALURU-27**

**SEMESTER EXAMINATION – APRIL 2017**

**B.Sc. Electronics – IV Semester**

**EL 415: Verilog HDL**

**Time: 90 Minutes Max. Marks: 35**

Note: The question paper has three parts and one printed page.

**PART – A**

**Answer any THREE of the following 03X05=15**

1. Why HDLs are important in digital designs? List the advantages and features of Verilog HDL.

2. Define a module in Verilog HDL. Explain different components of a module.

3. Explain different ways of specifying delay based time controls in Verilog procedural assignment statements with suitable example.

4. With example, explain the structured procedure statements used in Verilog.

5. Differentiate between functions and tasks and give examples for each.

**PART – B**

**Answer any THREE of the following 03X06=18**

6. Write a Verilog HDL design and test module for 4 to 1 multiplexer.

7. Write a design module and test module using behavioral modeling for d flipflop.

8. Write a verilog module (design and test) for 4 bit ripple carry counter.

9. a. Write a module using always statement to design a clock with time period = 10 and duty cycle = 40%. Initial value of clock = 0.

b. Write a module using repeat loop to delay the statement a = a+1 by 20 positive edges of clock.

10. Write a design and test module for 4 bit ripple carry adder.

**PART – C**

**Answer any TWO of the following 02X01= 02**

11. What is the difference between logical equality and case equality operators?

12. Find the values of sum, q and r after executing the following program.

a=4’b001x;b=4’b0100;d=6;e=4;f=2;

sum = a+b;

q=d/e;

r=e\*\*f;

13. What is the function of defparam statement in verilog.

14. Where *case* statement is used in Verilog HDL?

EL-415-B-17